A Proposal for I/O Pins Partitioning and Placement in 3D ICs

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Abstract

3D ICs is an upcoming technology to improve circuit wires. Physical Design of such circuits is a new research area, since many old problems changes and demand new solutions. Among these problems, the I/O pins of blocks must be mapped from a 2D initial arrangement to a 3D space. This paper presents a flow proposal that will lead to this problems solution. Files formats, parsers, algorithms and academic tools are discussed.

1. Introduction

In civil construction, buildings are a solution to the problem of accommodating large amount of people in big population centers. In addiction to allowing higher population densities, such structure improves the people concentration, mainly if the space is small. The VLSI submicron technology has similarities. Physical design is a very complex step that has to accommodate space for millions of cells and millions of wires connecting then. Wire congestion is a big issue. At the same time, wire delays are increasing dramatically. Many techniques are applied to alleviate wiring problems, such as buffering, sizing, congestion driven placement. However, these techniques are old and will not handle completely the upcoming wiring issues in the future designs. The advances of technology increases the wires delay compared to gates delay, while congestion becames even harder. The 3D VLSI [SAP 2005] is coming as one of the necessary changes of technology and design paradigm in order to break the wiring issues. Similarly to the civil construction, stacking the IC layers is a way to increase density and keep the elements close to each other, improving the circuit wires.

3D ICs have several advantages over 2D ICs including higher transistor packing densities and shorter interconnect lengths. On the other hand, 3D integration faces several problems as: (a) 3D vias are very big and resistive (it consumes several routing resources); (b) Thermal effects. At the same time, design tools have to change in order to cope with the new issues of 3D integration. Physical Design is responsible of partitioning the design in two or more active layers. The existing 2D tools will not be able to handle 3D effectively as 3D vias and thermal problems are big issues that cannot be ignored.

In this paper we focus on the problem of placing random logic blocks in several active layers. This kind of block has an I/O pin interface that connects it to the rest of a circuit. This interface is designed for a 2D fashion and usually the interface is the boundary to the area of the block. However, with the possibility of placing the block in more than one layer, the I/O pins must be partitioned in order to reduce the amount of pins in each layer and reduce the 2D area. Additionally, placement algorithms will be able to use the pins as a guide to the placement problem. The quadratic placement algorithm [ALP 1997], for instance, needs to have an I/O boundary to achieve convergence. A 3D extension of such an algorithm will need I/Os in the Z axis as well.

The remainder of this paper is organized as follows. In Section 2, we present an introduction for 3D VLSI. In Section 3, we describe 3D placement showing the problems and previous work. The Section 4 relates the I/O pins placement problems. In the Section 5, we propose a new flow that convert 2D format in tiers. Finally, in the section 6, we describe the algorithm to find the smaller logical path between pads. We present the conclusion the paper in Section 7.

2. 3D VLSI Circuits

The 3D ICs are made with the integration of several 2D ICs that are fabricated separately. The 2D ICs can be different in nature, like analog, MEMs, digital, processors, etc. There are many advantages of such fabrication, mainly because it is a promising change of paradigm to overcome the interconnect issues of recent ICs. 3D technology is actually a very promising new research area, since new solutions must come from system level design to physical level.

There is a massive interest from both industry and academia in 3D integration issues. Major companies like IBM, Intel, Samsung, Micron, Cadence and Infineon are some examples. There are also some very interesting work coming from startups, such as Ziptronix, Xanoptix and Tezzaron. From Academia, there is strong initiative from MIT, Cornell University, University of Minessotta, Stanford University, IMEC, Purdue University and Tohuku University. The 3D integration solutions comes from technology perspective (such as

copper bonding, SOI stacked layers, diffusion soldering, and others), design perspective (stacked memories, commercial solutions for stacked processor and memory) and CAD perspective (new algorithms and tools). More details can be found at Tezzaron home-page [TER 2006]. They provide a wide range picture of companies, universities and initiatives related to 3D ICs.

There are two integration strategies: face-to-back (face2back) and face-to-face (face2face), pictured in figure 1. In the face2back strategy, the chips are stacked one in the top of the other. In the top of the last metal layer of chip 1 (as in the example of figure 1 (a)) there is an insulation layer and then the bulk of chip 2. For the manufacturing of a 3D via, the insulator and the bulk must be etched and them metalized. The via will connect the last metal layer of chip 1 to the first metal layer of chip 2. In the face2face strategy, the chips are stacked in the face of the other (as in figure 1 (b)).

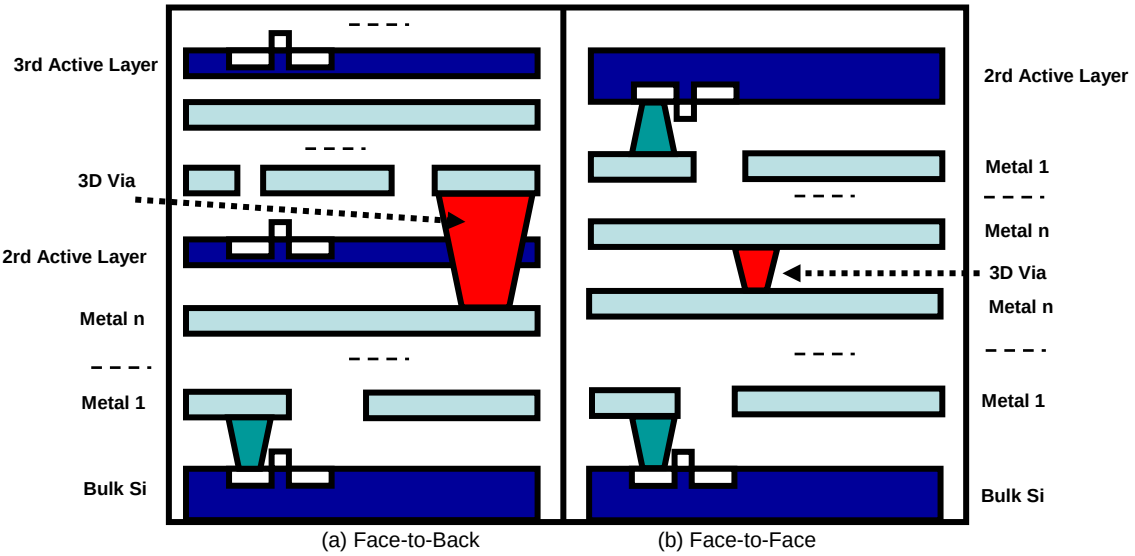

Figure 1: Face-to-Back and Face-to-Face 3D Integration Methods

3. 3D Placement

A 3D circuit can be organized by placing 2D macros in a stacked way, without breaking a block into two or more active layers. Intel and other major companies proposed, for example, to place the memory in one layer while the processor is placed in another layer, increasing memory bandwidth. On the other hand, a random logic block could be broken into two or more layers. The 3D placement problem, besides placing cells in the 2D space, should make the partitioning of the cells into different layers as show in figure 2. The 3D vias space should be properly allocated in order to guarantee that there will be enough space for vertical connections. The 3D placer should take advantage of the extended placement space to improve wire length, timing, area and power.

3.1. Previous Work

Goplen and Sapatnekar present in [GOP 2003] a force directed cell placer with thermal forces in order to improve chip temperature. The thermal forces move the cells away from high temperature zones. Additionally, there are attractive forces to the other cells and I/O pins of the same net. And repulsive forces to unmake cell overlaps.

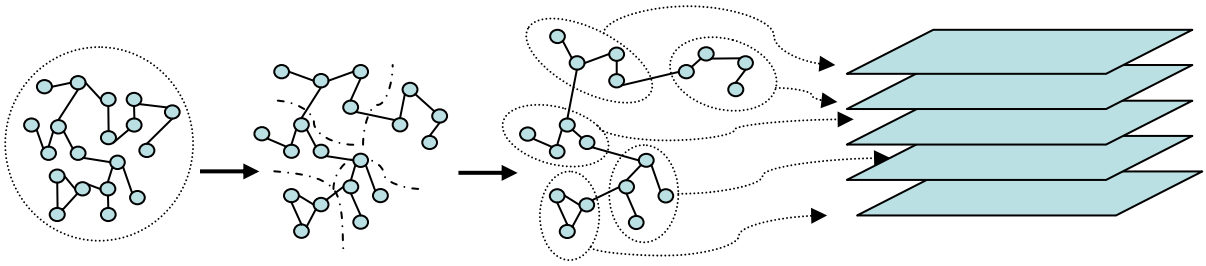

Figure 2: General idea for 3D ICs with 5 tiers

Kaya et. al in [KAY 2003] present their force directed 3D placer. It is similar to the one presented in the last paragraph, but it does not perform thermal optimization. Its repulsive forces are related to overlaps only. They mention in the paper that they consider 3D-Vias. However, their consideration is very simplistic, since all they do is to minimize the number of 3D-Vias.

Obenaus et. al, in [OBE 1999] present their force directed method for 3D placement. They define the 3D placement problem to minimize wire length only. Via costs and constrains are not considered. Gravity does not have repulsive forces. To solve overlaps, they have a Bucket Rescaling method that helps spreading cells on the chip.

Deng and Maly in [DEN 2001] , present their 3D cell placer based on Capo partitioning approach. Their paper purpose is not to propose a new placer, but to estimate wire lengths on a 3D IC compared to a 2D solution. The results show improvement, in wire length.

4. I/O Pins Partitioning and Placement

The I/O pins are fixed vertices locate in the edges of random blocks. It is responsible for external communication and for limiting the area (boundary). We raise two approaches related to I/O pins problem:

(a) Considering the initial position. In 2D ICs we have a "tip" of which pins must be placed together in the same tier.

(b) Not considering the physical information of I/O pins, but using the netlist instead.

Our work is based on the second approach. In this case, we use the *smallest logical path* criterion. Thus, we need to find closest pins and place them in different tiers. The I/O pins with smaller logical path will be kept in the same tier. This criterion considers the balance between tiers (related pads) and size of the area. The next sections we will present this approach in more details.

5. Flow Proposal

The figure 3 shows the 3D flow proposal. The input file is Bookself 2D format with fixed vertices (I/O pins). The second step determines the Pads position considering *the shortest logical path*. For this, we implement the BFS algorithm and create a new file with fixed vertices information. This information will be the input to the partitioner. We employ a *partitioning* step using hMetis algorithm [KAR 1997] to divide the circuit into a number of balanced partitions, equal to the number of tiers for 3D integration. The goal of this first min-cut is to minimize the connections between tiers, which translates into reducing the number of vertical wires and decreasing the area overhead associated with 3D vias. Thus, the Bookself format is converted to hMetis format in order to create the tiers. After the hMetis perform, a new file containing the cells and I/O pins information in different partitions is created. This file is input to the new conversion: hMetis format to Bookself format. The results are two files that contain informations about cells, I/O pins and tiers. In this step, we have the tiers, pads and cells. Finally, the pads physical positions are fixed in each tier and the cells are placing using a placer based on Quadratic Placement and Simulated Annealing [HEN 2006]. In this case, the placement is performed on each tier separately.

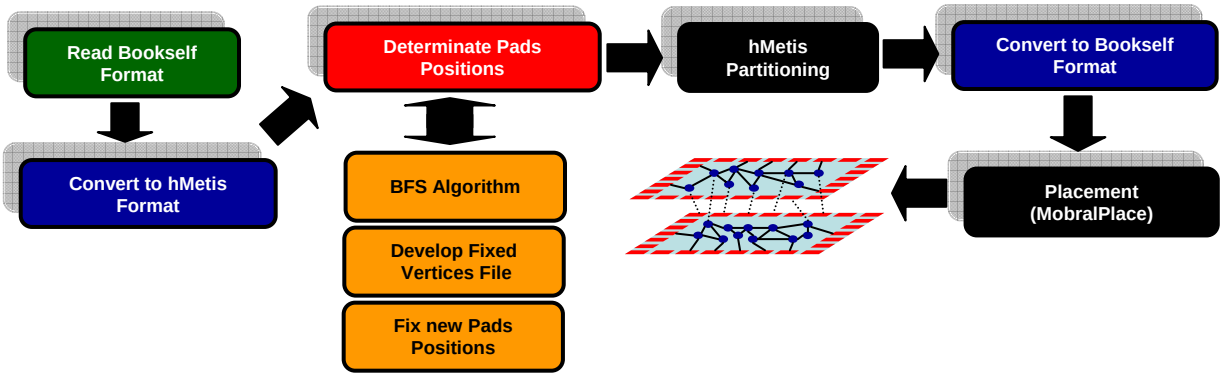

Figure 3: Proposal 3D I/O Pins Flow

6. Algorithm for Smallest Logical Path

In this paper, we provide a technique to partition I/O Pins between the partitions using *the smallest logical path* criterion. The BFS (Breadth-First Search) algorithm was used to locate the shortest logical path between two pins. All pads are compared in order to find the closest pins. For instance, the figure 4 show two combinations: BFS(A,G) and BFS(A,H). In the first combination, the path between pins A and G has length of 1 unit, while the path between pins A and H costs 5 units. This mean that (A,G) is logically closer than (A,H). The cost is measured through the number of the cells between save and target.

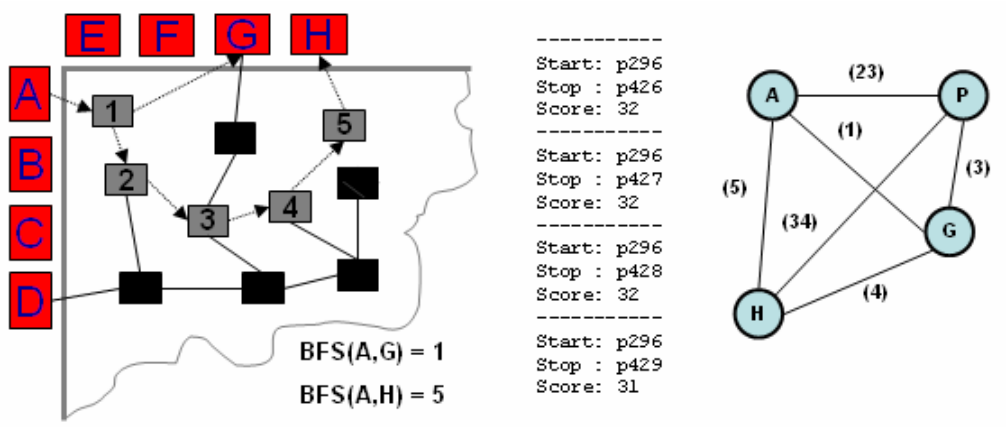

Figure 4: BFS Algorithm applied in the flow

The closest I/O pins will be candidates to stay in same tier. We create a complete graph of pins weighting the edges based on their logical distance. We keep the criterion of shortest logical path to determine the pads physical position in the different tiers. With the information about the pads location, the circuit is partitioned and cells are changed considering the min-cut between tiers.

7. Conclusion and Future Work

In this paper we discussed the I/O pins physical position problems and we presented a proposal of the solution based on *shortest logical path*. As future work we will implement the algorithms and make the validation of the proposed flow and exercise comparations with others possibilities. It is important to point out that 3D circuit is a brand new research area and preliminary experiments and flows are important advances.

8. References

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