Studying the Influence of I/O Pads Placement on Wirelength and 3D-Vias of VLSI 3D Integrated Circuits

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Abstract

Currently, most of the cells placers spread its cells guided by the I/O Pads position, for example, the quadratic placers. This paper studies the influence of I/O pads position on wirelenght and 3D-Vias of 3D integrated circuits. A method for I/O Pads partitioning and placement is proposed based on shortest logical path and extended to be applied for mixed-size blocks. Other approaches of I/O Pads targeting 3D integrated circuits are explored and described in this work.

1. Introduction

It is common sense that interconnects optimization is a huge issue for physical design algorithms. High delay, hard manufacturability, power, noise and crosstalk are some of the issues related to it.

3D circuits appear as a change of design paradigm, providing higher integration and reducing wire lengths [DAV 2005]. By either analytical methods [BAN 2001], [DAS 2004], [RAH 2000] and practical experimentation [DAS 2004], [DAV 2005], [ABA 2005], [KAY 2004], it is well known that 3D circuit technology has the potential of providing many improvements to VLSI circuits,

Among the new issues introduced by 3D circuits, the communication elements (known as 3D-Vias) between adjacent tiers impose several constraints to the physical design of those circuits. Firstly, their electrical characteristics are differentiated from regular wires. From the routing perspective, in order to connect to 3D-Via, a wire is required to cross all metal layers. More importantly, 3D-Vias require significant sizes for design rules such as minimum pitch. The face-to-back communication imposes more restrictions, since it digs a hole through the Bulk of a tier occupying active area and compromising reliability. All those factors make 3D-Via planning a complex issue that must be addressed by CAD tools.

The new 3D issues must be addressed with proper CAD tools able to synthesize in a new design paradigm to take full advantage of 3D integration. Among possible design methodologies, the integration granularity will impact possible benefits and the type of problems to be solved. Initially consider a tier level integration, which stacks separated tiers of different nature. It is the most coarse level granularity and do not severely affect existing design methodologies, since each tier can be designed separately with a simple glue logic to integrate them. Secondly, consider an ip core level integration that partitions big circuit blocks (ip cores) into different tiers, providing a tighter integration (more communication between tiers). Finally, random logic level partitioning breaks random logic into 3D. Basically, the finer the integration grain is, bigger it is the potential requirement for vertical communication, causing two effects: 1) more potential benefits; 2) more complex 3D-Via related problems to solve. The higher complexity of 3D-Via planning must be addressed by physical design algorithms, encouraging research on this field. The random logic integration granularity with the usage of more 3D-Vias while optimizing wire length of a block on 3D leads to a better usage of the 3D resources and helps reducing wire length, as demonstrated by [DAS 2004].

This paper proposes a study of the influence of I/O Pads placement on wirelength and 3D-Vias of VLSI 3D integrated circuits. A method for I/O Pads partitioning and placement is proposed based on shortest logical path. The remainder of this paper is organized as follows. In Section 2, we describe related works showing the problems and solutions. The Section 3 shows some I/O Pads structures. The Section 4 relates the plan of proposed method for I/O Pads partitioning and placement. Finally, we present the conclusion and future works the paper in Section 5.

2. Related Works

Because of the high penalties imposed by 3D-Vias, a common approach in the placement phase is to minimize them by using min-cut partitioning. The works from [DAV 2005], [ABA 2005] for instance, apply min-cut partitioning (usually with hMetis tool [KAR 1999]) to assign cells into tiers, minimizing the number of 3D-Vias. A subsequent step performs 2D placement on each tier separately; the already placed tiers can serve as a guide to subsequent tiers in order to minimize wire length. However, [KAY 2004], [LIU 2005], [DAS 2003] already identified that this approach leads to worse results in terms of wire length. We call True 3D placer a method that is able to both measure and optimize wire length in all the axis at the same time.

Liu et. al [LIU 2005] built a two step 3D placement flow similar to the one mentioned above using hMetis for partitioning the cells into tiers. They argue that building a True 3D flow is very hard and for this reason they concentrate on improving the partitioning step. They observed that the insertion of 3D-Vias could potentially improve wire length. For this reason, their cell partition does not perform min-cut partitioning, but tries to maximize the 3D-Vias under an upper bound constraint. In fact, since face-to-face integration allows 3D-Vias with no cost to yield or area, they could be inserted freely in order to improve wire length. Some preliminary evaluation could be performed to analise a reasonable upper bound for those 3D-Vias. Liu's algorithm cannot achieve the exact via count provided, but tries to get a close approximation by an iterative algorithm.

Das et. al [DAS 2004] built a true 3D partitioning based on placement engine. It recursively cuts the placement cube performing min-cut partitioning. A wire length and 3D-Via trade-off can be obtained by controlling the point at which the cut is performed into the Z axis (i.e. the point at which the design is partitioned into tiers). The optimal solution for wire length is obtained when the aspect ratio drives the cut direction.

Goplen and Sapatnekar [GOP 2003] formulate the 3D placement problem as a True 3D placement. They provide an analytical force directed algorithm that minimizes the squared 3D wire length. Their method is iterative; at each iteration repulsive forces related to thermal issues or cell overlaps are inserted in the system. The authors do not detail how they handle I/Os into the tiers; however, on quadratic placement methods the cells will not move in the Z axis unless the I/Os are placed in different tiers. In this case, it can be understood that the repulsive forces are responsible for moving cells into other tiers. After placement is completed, the cells are sorted in the Z axis and finally assigned to a circuit tier. This method may fall into a false wire length optimization since actually cells cannot be placed into continuous coordinate; the rounding of their coordinated could potentially decrease circuit wire length.

Obenaus et. al, in [OBE 1999], present an iterative force directed method for 3D placement. Different from Goplen's placer, it is not an analytical method but moves all cells (cell-by-cell) to an optimal position according to its connections. They define the 3D placement problem to minimize wire length only, which handles the problem as true 3D method. 3D-Via costs and constrains are not considered.

In preview works in [SAW 2006] [SAW 2006a], we presented a method for I/O pins partitioning targeting random logic based on the shortest logical path. This approach demonstrated good effectiveness both in terms of I/O balance and resultant number of 3D-Vias, outperforming both algorithms in both metrics.

3. I/O Pads Structure

The I/O Pads can be placed in several points of the circuit. For instance, the Tezzaron Technology [GUP 2005] place I/O Pads at the top and bottom layer of the circuit, as illustrated in the figure 1(a). In academia, Davis in [DAV 2005] and Kaya in [KAYA 2004] consider the I/O Pads at the top layer of the circuit. However, these works do not describe information about this issue. We are assuming that the authors are using simplistic approaches to place I/O Pads. To the authors' knowledge, there is no existing work that address placement of I/O Pads in 3D circuits. Therefore, this subject needs more investigation.

Figure 1(a) illustrates the I/O Pads placed at the top and bottom layer of the circuit. For instance, in this situation, the I/O Pads arrangement influences the subsequent placement of the cells because they are attracted by the Pads position. This fact can significantly modify the wirelength of the circuit. Another idea is illustrated in figure 1(b); it shows the I/O Pads distributed among the tiers. Both approaches need connections from blocks and cells to I/O Pads and each arrangement can will influence the cell placement quality differently. In this paper, we are addressing the I/O Pads placement and study the influence it has on the cell placement wirelenght and number of 3D-Vias.

In this context, the objectives of the work are: (a) to evaluate the influences of I/O Pads on the quality of wirelenght and number of 3D-Vias; (b) to propose a method to I/O Pads partitioning and placement.

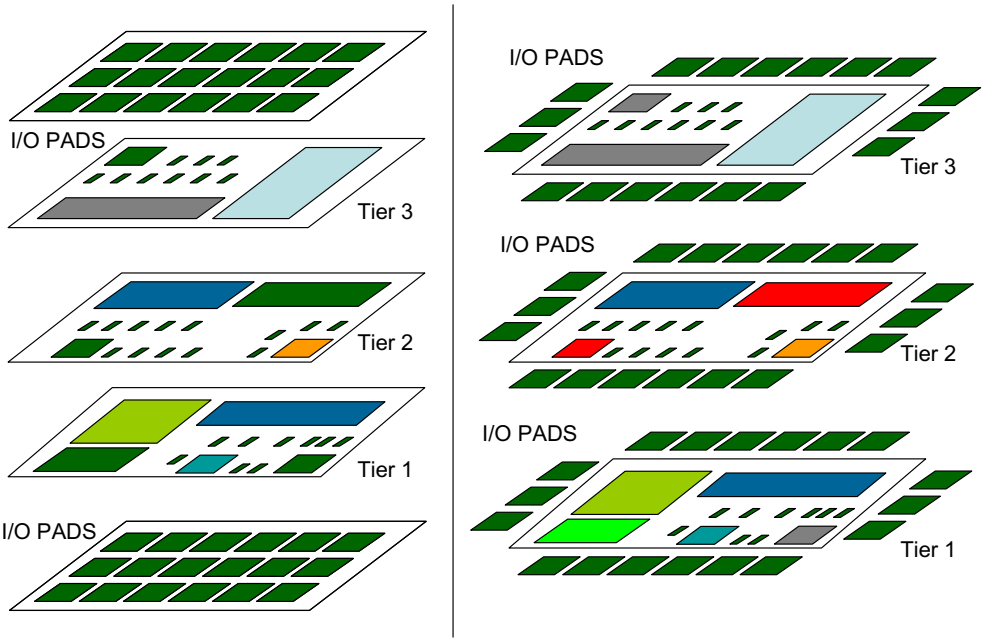

Figure 1. This picture illustrates two I/O PADS position forms. (a) I/O PADS placement at the top and bottom layer. (b) I/O PADS distributed among tiers.

4. Method Proposed

Currently, most cell placers spread the cells guided by the I/O Pads position. Therefore, the Pads position guides the connection to the blocks and cells of the circuit while reduces the wirelenght, area and number of 3D-Vias.

The methodology proposed can be evaluated using some strategies as: (1) to place blocks sequentially or concurrently with the I/O Pads placement; (2) to place I/O Pads at the top layer of the circuit or top and bottom layer of the circuit; (3) to distribute I/O Pads among tiers.

The I/O Pads algorithm constraints are: (a) PADS partitioning must consider the blocks before or after its placement. In this case, the method can contain information of the circuit before the blocks placement or simply place the pads and leave the placer free to find the best arrangement for the blocks. (b) the Pads partitioning must be flexible. The pads can be fixed to the top layer of the circuit or fixed to the top and bottom layer, or only distributed among the tiers.

All these possibilities must evaluate the reduction of wirelenght and number of 3D-Vias. After the evaluation the best arrangement of pads for each circuit can be found.

Figure 2. This picture illustrates the blocks and cells guided by the I/O Pads.

5. Conclusions and Future Works

In this paper we discussed the I/O Pads physical position problems and its influence on wirelenght quality. We presented some criteria to develop a method for I/O Pads partitioning and placement to be applied to mixed-size blocks of 3D integrated circuits. As future work we will implement the algorithms and make the validation of the proposed flow and compare to others possibilities.

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